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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,195	12/15/2003	Kwun Yao Ho	025796-00014	4785

7590 06/29/2006

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EXAMINER	
BRYANT, DELORIS S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,195	HO ET AL.	
	Examiner	Art Unit	
	Deloris Bryant	2813	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tijima et al (US 2001/0008309) in view of Taniguchi et al (US 6,404,062). Tijima discloses a semiconductor substrate having a first surface and a second surface (Fig. 3; lower and upper surface of 201, respectively); an insulating layer (Fig. 3; 202) being on said first surface; a multilayer interconnection structure (Fig. 3; lower half of 211) being on said insulating layer and having a third surface having a plurality of first bonding pads and a fourth surface having a plurality of second bonding pads (Fig. 9c; 203) and contacting

said insulating layer (Fig. 9c; 202); a plurality of conductive plugs (Fig. 3; 201a-b) penetrating said semiconductor substrate (Fig. 3; 201)and said insulating layer (Fig. 3; 202) and electrically connecting to said second bonding pads respectively (Fig. 3); a plurality of third bonding pads (Fig. 3; 203b and 203d) being on said second surface (Fig. 3; upper surface of 201) and connecting to said conductive plugs respectively (Fig. 3). Although Tijima only discloses a single chip connecting to said third bonding pads (Fig. 3; 203b and 203d), those of skill in the art will understand that device can contain duplication of parts (i.e. more that one chip component). See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) (Duplication of parts). Taniguchi teaches the use of plurality of chips. It would have been obvious to one skill in the art at the time of the invention to use the plurality of chips as taught by Taniguchi with the invention of Tijima for the advantage that the electrical performance of the package is improved.

Regarding claim 7, Tijima discloses wherein said chip individually and electrically connect to said third bonding pads (Fig. 3; 203b and 203d).

4. Claims 2-3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tijima et al (US 2001/0008309) in view of Taniguchi et al (US 6,404,062) and in further view of Tsunashima (US 6,383,837). Tijima and Taniguchi discloses the claimed invention as set forth above but fails to disclose wherein said multilayer interconnection structure includes at least one integrated circuit device (claim 2); wherein said semiconductor substrate has a thickness between 10 to 500 micron meter (claim 3); and that the first and second multichip module structure has the same

structure (claim 11). Tsunashima discloses a multilayer interconnection structure includes at least one integrated circuit device (col. 1, lns 20-48) and that the hole in the silicon substrate is 100 μm (col. 6, 46-54), which indicated that the thickness of the substrate is at least 100 μm which falls within the range indicated by the applicant. Tsunashima also discloses that the multiple structures can be of the same structure (col. 4, lns 13-64). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the structure taught by Tsunashima to produce a device that is small in area, simple in structure and small in thickness.

5. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tijima et al (US 2001/0008309) in view of Taniguchi et al (US 6,404,062) and in further view of Juskey et al (US 6,356, 453). Tijima and Taniguchi discloses the claimed invention as set forth above and although Tijima only discloses a single chip connecting to said third bonding pads (Fig. 3; 203b and 203d) and Taniguchi teaches the use of plurality of chips. Both Tijima and Taniguchi fails to teach the use of a passive and active chip (claim 4, 6). Juskey teaches that a multi-chip module includes a passive and active chip (col. 5, lns 59-60). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to provide an active and passive chip to be included in the multi-chip module structure for the benefit of using a must less costly technique.

6. Regarding claim 5, Tijima and Juskey disclose the claimed invention as set forth above but fails to disclose a flip-chip mounting process. Taniguchi teaches a flip-chip

mounting process (col. 1, lns 41-51). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the flip-chip mounting process of Taniguchi with the passive and active chip from Juskey so that connecting reliability can be ensured.

7. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tijima et al (US 2001/0008309) in view of Taniguchi et al (US 6,404,062) and in further view of Peterson et al (US 6,384,473). Tijima and Taniguchi discloses the claimed invention as set forth above but fails to disclose a first chip mounted on a second surface by flip-chip type and a second chip electrically connecting and stacking on a backside of first chip. Peterson, however, does teach a chip (Fig. 3A; 100) attached to a second surface (Fig. 3A; 18) by flip-chip type and a second chip (Fig. 5; 102) connected to the backside of the first chip (col. 12, lns 1-12). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to mount the chips by flip-chip type because of the many benefits including increased packaging density, thinner package height and electrical circuit interconnection.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tijima et al (US 2001/0008309) in view of Taniguchi et al (US 6,404,062) and in further view of Hirano et al (US 5,625,298). Tijima and Taniguchi disclose the claim limitations as set forth above but fails to disclose that the MCM structure is electrically connected with a package substrate. Hirano does disclose a MCM structure connected with a package

substrate (col. 1, lns 37-39). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to take the package substrate of Hirano and combine it with the teachings of Tijima to afford good dimensional stability throughout processing and good electrical characteristics.

Response to Amendment

9. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deloris Bryant whose telephone number is (571) 272-8670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

dsb

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